CLAIMS:

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1. An apparatus, comprising:

a first storage to store a plurality of data, said first storage coupled to a host bus through a first path and responsive to one or more of a plurality of control signals to transfer selected parts of said data to said host bus; and

a monitor circuit, coupled to said host bus to track processor initiated host bus cycles and to identify processor initiated host bus read cycles targeted to a virtual PCI device logically residing behind a primary PCI bus, wherein said primary PCI bus is coupled to said host bus through a second path which is distinct from said first path;

wherein said monitor circuit is to generate said plurality of control signals to transfer a select one or more said data to said host bus during one or more of said identified host bus read cycles targeted to said virtual PCI device.

2. The apparatus of claim 1, wherein said virtual PCI device is a virtual PCI-PCI bridge.

3. The apparatus of claim 1, further comprising a second storage coupled to said host bus and responsive to one or more of said plurality of control signals to selectively receive said data from said host bus to store in said second storage;

wherein said virtual PCI device resides logically behind a virtual PCI-to-PCI bridge which resides logically behind said primary PCI bus; and

wherein said monitor circuit is to further identify host bus write cycles targeted to a location, within a configuration space reserved for said virtual PCI-to-PCI bridge, which

specifies a bus number and to generate said control signals to receive said bus number from said host bus to store in said second storage.

4. The apparatus of claim 1, further comprising a processor which is coupled to said host bus, wherein said processor, said first storage, and said monitor circuit are integrated into a single chip package.

5. The apparatus of claim 3, wherein said first storage and said monitor circuit are coupled to said host bus through an internal processor bus.

6. The apparatus of claim 1, wherein said first storage is responsive to one or more of said plurality of control signals to selectively receive data from said host bus to store in said first storage;

wherein said monitor circuit is to further identify processor initiated host bus write cycles targeted to said virtual PCI device residing logically behind said primary PCI bus;

wherein said monitor circuit is to generate said plurality of control signals to receive data from said host bus to store in said storage during one or more of said identified host bus write cycles targeted to said virtual PCI device.

7. The apparatus of claim 1, wherein said storage is comprised of random access memory; and

said identified host bus read cycles targeted to said virtual PCI device include host bus cycles targeted to memory address space allocated to said virtual PCI device.

8. The apparatus of claim 1, further comprising a mirror register coupled to said host bus and responsive to one or more of said control signals to receive data from said host bus;

wherein said monitor circuit is to further identify host bus write cycles targeted to a configuration-address register; and

wherein said monitor circuit is to generate said control signals to receive data from said host bus to store in said mirror register during said host bus cycles identified as targeted to said configuration-address register.

9. The apparatus of claim 1, wherein said identified host bus read cycles targeted to said virtual PCI device include host bus cycles to I/O address space allocated to said virtual PCI device.

10. The apparatus of claim 1, wherein said first storage includes a first plurality of configuration registers; and

wherein said identified host bus cycles include host bus cycles targeted to configuration space reserved for said virtual PCI device.

11. The apparatus of claim 10, wherein said virtual PCI device resides behind a virtual PCI-to-PCI bridge, and

wherein said first storage includes a second plurality of configuration registers,

and wherein said monitor circuit is to further identify host bus cycles targeted to configuration space allocated to said virtual PCI-to-PCI bridge, and

wherein said monitor circuit is to generate said plurality of control signals to transfer a select one or more said data to said host bus during one or more of said identified host bus read cycles targeted to said configuration space allocated to said virtual PCI-to-PCI bridge.

12. An apparatus, comprising:

a first storage, wherein contents of said first storage specify a first address space allocated to a primary PCI bus.

a second storage, wherein contents of said second storage specify a second address space allocated to a virtual PCI device logically residing behind said primary PCI bus; and

a control circuit, coupled to said first and said second storage, wherein said control circuit is to couple to a host bus to track processor initiated host bus cycles and to select host bus cycles to route to said primary PCI bus, wherein said routed cycles are to be selected, based on said contents of said first storage and said second storage, to exclude host bus cycles targeted to said second address space.

13. The apparatus of claim 12, wherein said first and said second address space includes memory host bus address space.

14. The apparatus of claim 12, wherein said first and said second address space includes host bus I/O space.

15. The apparatus of claim 12, wherein said first and said second address space includes PCI compliant configuration address space.

16. The apparatus of claim 12, wherein said virtual PCI device is a virtual PCI-to-PCI bridge.

17. The apparatus of claim 16, further comprising:

a plurality of configuration registers;

a third storage coupled to said control circuit, wherein contents of said third storage indicate a bus and a device number in which said virtual PCI-to-PCI bridge logically resides, and wherein said control circuit is to further select, based on said bus and said device number, host bus cycles, targeted to configuration address space of said virtual PCI-to-PCI bridge, to route to said plurality of configuration registers.

18. A system comprising:

one or more processors coupled to a host bus;

a host-to-PCI bridge to route select processor initiated host bus cycles to a primary PCI bus; and

a host bus device, coupled to said host bus, to monitor said host bus, to identify processor initiated host bus cycles targeted to a first virtual PCI device which resides logically behind said primary PCI bus, and to intercept select said identified cycles targeted to said first virtual PCI device;

wherein said host-to-PCI bridge is to not forward said identified cycles which are targeted to said first virtual PCI device.

19. The system of claim 18, wherein said first host bus device includes a plurality of configuration registers, wherein said intercepted cycles, include host bus cycles targeted to configuration space reserved for said first virtual PCI device and are to be routed to access said plurality of configuration registers.

20. The system of claim 18, wherein said first host bus device includes an array of memory devices, wherein said intercepted cycles include host bus cycles targeted to a memory space allocated to said virtual PCI device and are to be routed to access said array of memory devices.

21. The system of claim 18, further comprised of a second host bus device coupled to said host bus, wherein each said host bus device intercepts host bus cycles targeted to a distinct virtual PCI device which resides logically behind said primary PCI bus, wherein said distinct virtual PCI devices each have a distinct bus number and device number combination.

22. The system of claim 18, wherein said virtual PCI device resides logically behind a primary virtual PCI-to PCI bridge, wherein said primary virtual PCI-to-PCI bridge resides logically behind said primary PCI bus, and wherein said host bus device is to snoop said host bus to determine a bus number assigned to said primary virtual PCI-to PCI bus.

23. The system of claim 22, wherein said virtual PCI device resides logically behind a secondary virtual PCI-to PCI bridge which resides logically behind said primary virtual PCI-to-PCI bridge; and

wherein said first host bus device includes a plurality of bridge configuration registers, wherein said intercepted cycles include host bus cycles targeted to the configuration space reserved for said secondary virtual PCI-to PCI bridge and are to be routed to access said plurality of bridge configuration registers.

24. A method comprising:

capturing a current host bus cycle initiated by a processor;

determining whether said captured cycle is targeted to a virtual PCI device residing logically behind a primary PCI bus; and

intercepting said current host bus cycle, if said current cycle is determined to be targeted to said virtual PCI device, and not routing said cycle to said primary PCI bus.

25. The method of claim 24, wherein said intercepting includes routing to access a storage coupled to said host bus.

26. The method of claim 24, wherein said intercepting includes routing to access a location within a plurality of configuration registers.

27. The method of claim 24, wherein said determining includes determining whether said current cycle is a write cycle targeted to a configuration-address register and snooping said current host bus cycle to receive data from said host bus if said current cycle is a write cycle targeted to said configuration-address register and writing some or all of said data into a mirror register.

28. The methods of claim 24, wherein said determining includes determining whether said current cycle is a write cycle targeted to a location within the configuration registers of a virtual primary PCI-to-PCI bridge in which a bus number is specified; and

snooping said current host bus cycle to receive data from said host bus if the current cycle is a write cycle to a location within the configuration registers of a virtual primary PCI-to-PCI bridge in which a bus number is specified and writing said data in a storage.

29. The method of claim 24, wherein said determining includes determining whether said cycle is to a location within the configuration registers of a virtual PCI-to-PCI bridge; and

intercepting said current host bus to route to access a location within a plurality of bridge configuration registers if said cycle is to a location within the configuration registers of a virtual PCI-to-PCI bridge.

30. The method of claim 24 wherein said virtual PCI device is a virtual PCI-to-PCI bridge